4.5 Gb, DDR3, 64 M x 72 Integrated Module (IMOD)

FEATURES

- DDR3 Integrated Module [iMOD]:
  - Vcc=VccQ=1.5V ± 0.075V
  - 1.5V center-terminated, push/pull I/O
  - Package: 25mm x 25mm, 16 x 16 matrix w/ 255 balls
  - Matrix ball pitch: 1.00mm
- Space saving footprint
- Thermally enhanced, Impedance matched, integrated packaging
- Differential, bidirectional data strobe
- 8n-bit prefetch architecture
- 8 internal banks (per word, 9 Bytes integrated in package)
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals.
- CAS (READ) latency (CL): 6, 8, and 10
- CAS (WRITE) latency (CWL): 6, 7 and 8
- Fixed burst length (BL) of 8 and burst chop (BC) of 4
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self/Auto Refresh modes
- Operating Temperature Range (Case Temp=Tc)
  - Industrial: -40˚C to 85˚C supporting SELF & AUTO REFRESH
  - Extended: -40˚C to 105˚C; manual REFRESH only
  - Mil-Temp: -55˚C to 125˚C; manual REFRESH only
- CORE clocking frequencies:
  - Industrial: 667MHz, 533MHz and 400MHz
  - Extended: 533MHz and 400MHz
  - Mil-Temp: 400MHz
- Data Transfer Rates:
  - Industrial: 1333, 1066 and 800 Mbps
  - Extended: 1066 and 800 Mbps
  - Mil-Temp: 800 Mbps
- Write leveling
- Multipurpose register
- Output Driver Calibration

Benefits

- 20% space savings while providing a surface mount friendly pitch (1.00mm)
- Reduced I/O (46%)
- 25% improvement in routings for your memory array
- Reduced trace lengths due to the highly integrated, impedance matched packaging
- Thermally enhanced packaging technology allow silicon integration without performance degradation due to power dissipation (heat)
- High TCE organic laminate interposer for improved glass stability over a wide operating temperature
- Suitability of use in High Reliability applications requiring Mil-temp, non-hermetic device operation

*Note: This integrated product is currently under consideration. Latest product status, information, and/or corresponding documents should be obtained from LDI prior to your design considerations.

iMOD Part Information

Order Number	Speed Grade	Device Grade	Pkg Footprint	I/O	Pitch	Pkg No.
L9D345G72BG5I15	DDR3-1333	Industrial	25mm x 25mm	255	1.00mm	BG5
L9D345G72BG5E19	DDR3-1066	Extended				
L9D345G72BG5M25	DDR3-800	Mil-Temp				

iMOD
integrated module products

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Integrated vs. Monolithic Solutions - highlights

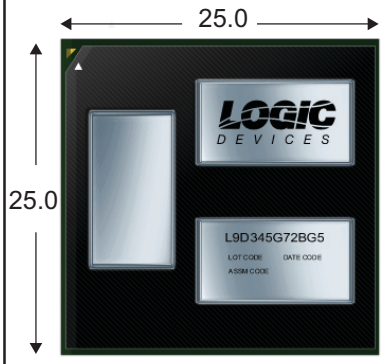
OPTIONS	Monolithic Solution	IMOD Solution	SAVINGS
			
Area	5 x 139.5mm^2 + component space = ~775mm^2	625 mm^2	~20%
I/O	5 x 96 pins = 480 pins total	255 Balls/Locations	46%

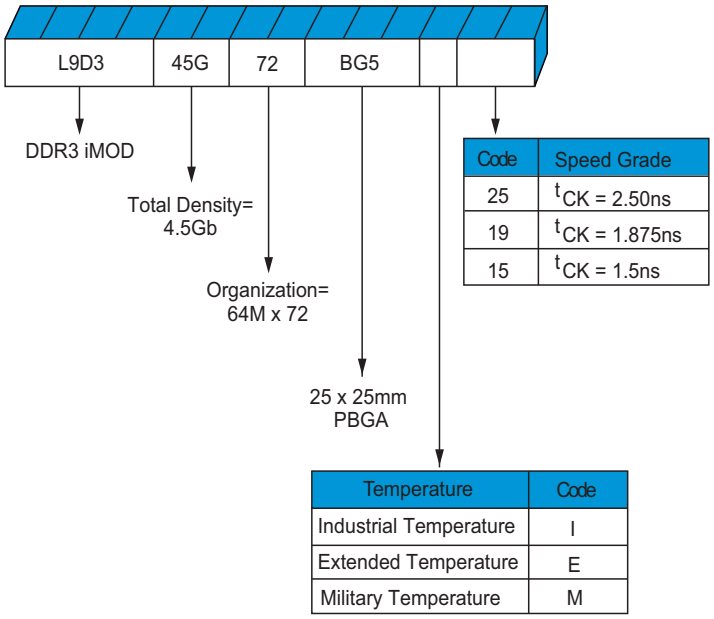
Table 1: Key Timing Parameters

Device Grade	Speed Grade	Speed Mark	Part Ordering Information	CORE Freq. [MHz] Support	Data Rate [Mbps] Support	Target ^{t}RCD-^{t}RP-CL	^{t}RCD [ns]	^{t}RP [ns]	CL [ns]
INDUSTRIAL	DDR3-1333	15	L9D345G72BG5I15	667/533/400	1333/1066/800	10-10-10/8-8-8/6-6-6	15	15	15
EXTENDED	DDR3-1066	19	L9D345G72BG5E19	533/400	1066/800	8-8-8/6-6-6	15	15	15
MIL-TEMP	DDR3-800	25	L9D345G72BG5M25	400	800	6-6-6	15	15	15

FEATURES

FIGURE 1 - 1Gb DDR3 PART NUMBERS

Sample Part Number: L9D345G72BG5M15



Code	Speed Grade
25	^{t}CK = 2.50ns
19	^{t}CK = 1.875ns
15	^{t}CK = 1.5ns

Temperature	Code
Industrial Temperature	I
Extended Temperature	E
Military Temperature	M

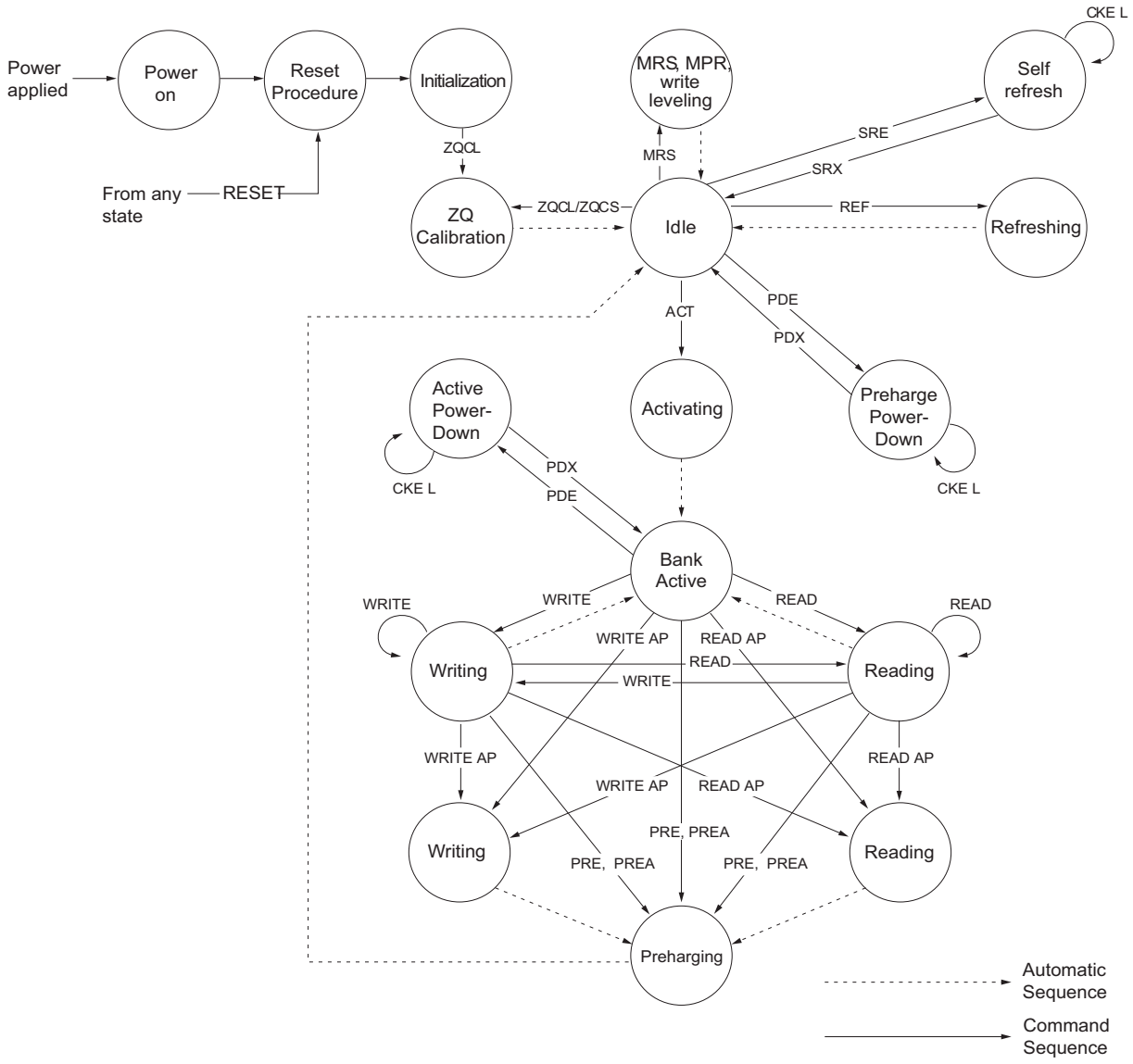
Note: Not all options can be combined. Please see our Part Catalog for available offerings.

TABLE 2: ADDRESSING

Parameter	64 Meg x 72
Configuration	[8 Meg x 8 banks x 16] x 4.5
Refresh Count	8K
ROW Addressing	8K (A[12:0])
Back Addressing	8 (BA[2:0])
Column Addressing	1K (A[9:0])

STATE DIAGRAM

FIGURE 2 - SIMPLIFIED STATE DIAGRAM



ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE
PREA=PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry
SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

FUNCTIONAL DESCRIPTION

The DDR3 SDRAM uses double data rate architecture to achieve high speed operation. The double data rate (DDR) architecture is an 8n prefetch with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE access for the DDR3 SDRAM consists of a single 8n-bit-wide, one-clock-cycle data transfer at the internal memory core and eight corresponding n-bit-wide, one-half-clock-cycle data transfer at the I/O pin.

The differential strobes (LDQSx, LDQSx\, UDQSx, UDQSx\) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The READ data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CKx, CKx\). The crossing of CK going HIGH and CK\ going LOW is referred to as the positive edge of Clock (CK). Control, Command, and Address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

READ and WRITE accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and the starting column location for the burst access.

DDR3 SDRAM devices use READ and WRITE BL8 and BC4. An AUTO PRECHARGE function may be enabled to provide a self-timed ROW PRECHARGE that is initiated at the end of the burst access.

As with standard DDR SDRAM devices, the pipelined, multi-bank architecture of the DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding ROW PRECHARGE and ACTIVATION time.

A SELF REFRESH mode is provided for all temperature grade offerings along with AUTO SELF REFRESH for Industrial product, as well as, power-saving, POWER-DOWN mode.

INDUSTRIAL TEMPERATURE

The industrial temperature (I) device requires the case temperature not exceed -40˚C or +85˚C. JEDEC specifications require the REFRESH rate to double when Tc exceeds +85˚C; this also requires use of the high-temperature SELF REFRESH option. Additionally, ODT resistance and the INPUT/OUTPUT impedance must be derated when the Tc is <0˚C or >+85˚C.

EXTENDED TEMPERATURE

The Extended temperature (E) device requires the case temperature not exceed -40˚C or +105˚C. JEDEC specifications require the refresh rate to double when Tc exceeds +85˚C; this also requires use of the high-temperature SELF REFRESH option. Additionally, ODT resistance and the INPUT/OUTPUT impedance must be derated when the Tc is <0˚C or >85˚C.

MILITARY, EXTREME OPERATING TEMPERATURE

The Mil-Temp (M) device requires the case temperature not exceed -55˚C or +125˚C. JEDEC requires the REFRESH rate double when Tc exceeds +85˚C and LDI recommends an additional derating as specified in this document as to properly maintain the DRAM core cell charge at temperatures above Tc>105˚C.